गोंय विद्यापीठ
ताळगांव पठार,
गोंय – ४०३ २०६
फोन : +९१-८६६९६०९०४८

International Year of Cooperatives
Cooperatives Build a Better World

(Accredited by NAAC)

Goa University
Taleigao Plateau, Goa-403 206
Tel : +91-8669609048
Email : registrar@unigoa.ac.in
Website : www.unigoa.ac.in

GU/Acad –PG/BoS -NEP/2025-26/294 Date: 06.08.2025

CIRCULAR

The Academic Council & Executive Council of the University has approved Ordinance OA-35A relating to PG Programmes offered at the University campus and its affiliated Colleges based on UGC 'Curriculum and Credit Framework for Postgraduate Programmes'. Accordingly, the University has proposed introduction of Ordinance OA-35A from the Academic year 2025-2026 onwards.

The Programme structure and syllabus of Semester I and II of the **Master of Science in Electronics** Programme approved by the Standing Committee of the Academic Council in its meeting held on 24th & 25th June 2025 is attached.

The Dean & Vice-Dean (Academic) of the School of Physical and Applied Sciences are requested to take note of the above and bring the contents of the Circular to the notice of all concerned.

ASHWIN VYAS LAWANDE
Digitally signed by ASHWIN VYAS LAWANDE
Date: 2025.08.06 15:06:16 +05'30'

(Ashwin V. Lawande)
Deputy Registrar – Academic

To,
1. The Dean, School of Physical and Applied Sciences, Goa University.
2. The Vice-Dean (Academic), School of Physical and Applied Sciences, Goa University.

Copy to:
1. Chairperson, BoS in Electronics, Goa University.
2. Programme Director, M.Sc. Electronics, Goa University.
3. Controller of Examinations, Goa University.
4. Assistant Registrar Examinations (PG), Goa University.
5. Director, Directorate of Internal Quality Assurance, Goa University for uploading the Syllabus on the University website.

GOA UNIVERSITY

MASTER OF SCIENCE IN ELECTRONICS

(Effective from the Academic Year 2025-26)

ABOUT THE PROGRAMME

The School of Physical and Applied Sciences is a result of the amalgamation of three correlated departments which belonged to the erstwhile Faculty of Natural Sciences. Department of Electronics, on the other hand, was established in 2010, centred around the M.Sc. Electronics programme started by the Physics department in 1992.Department of Electronics was identified by UGC to initiate Innovative program in Embedded Technologies. The success of the program is a result of the foundations of a vibrant academic culture and significant contributions of several of our distinguished personalities.

OBJECTIVES OF THE PROGRAMME

Presently the thrust area of the program is in areas of embedded system, agro-electronics, Signal and Image processing and Smart instrumentation. The main objectives of the curriculum are to train and have hand-on experience for the pupil in the area of embedded technologies having application in data communication, signal, image processing and smart instrumentation so that they are employable in the industry.

PROGRAMME SPECIFIC OUTCOMES (PSO)

PSO 1.	**Gain profound knowledge** about Embedded systems, the Internet of things (IoT), Artificial Intelligence (AI) and Electric vehicles technology.
PSO 2.	**Implementing the experiments** on Embedded systems, Programmable logic, IP cores like soft-core processors, having applications in Control systems & Robotics, Smart Sensors instrumentation, and Biomedical.
PSO 3.	**Applying the concepts** of signals-system and various Machine learning techniques for applications like agro-electronics, Image processing, Neural system, Biomedical etc.
PSO 4.	**Analysing performance metric** of Machine learning algorithms and various embedded platforms.
PSO 5.	**Developing a technological solution** to societal problems by utilizing state-of-theart technologies.

Approved by: Standing Committee of the Academic Council on 24th & 25th June 2025

PROGRAMME STRUCTURE
Master of Science in Electronics
Effective from Academic Year 2025-26

Bridge Course			
Sr. No.	**Course Code**	**Title of the Course**	**Credits**
1	ELE-1000	Introduction to Electronics	02

Semester I				
Discipline Specific Core (DSC) Courses (16 credits)				
Sr. No.	**Course Code**	**Title of the Course**	**Credits**	**Level**
1	ELE-5000	Micro Electronics and VLSI Design	4T	400
2	ELE-5001	Signals and Systems	4T	400
3	ELE-5002	Embedded System Design	4T	400
4	ELE-5003	Electronics Practicals-I	4P	400
		Total Credits for DSC Courses in Semester I	**16**	
Discipline Specific Elective (DSE) Course (4 credits)				
Sr. No.	**Course Code**	**Title of the Course**	**Credits**	**Level**
1	ELE-5201	EDA Tools	2T	400
2	ELE-5202	EDA Tools Lab	2P	400
3	ELE-5203	Numerical Computation and Algorithms	2T	400
4	ELE-5204	Numerical Computation and Algorithms Lab	2P	400
		Total Credits for DSE Courses in Semester I	**4**	
		Total Credits in Semester I	**20**	

Semester II				
Discipline Specific Core (DSC) Courses				
Sr. No.	**Course Code**	**Title of the Course**	**Credits**	**Level**
1	ELE-5004	Advanced Digital Communication System	4T	500
2	ELE-5005	Real Time Operating Systems	4T	500
3	ELE-5006	Digital System Designs	4T	500
4	ELE-5007	Electronics Practicals-II	4P	500
Total Credits for DSC Courses in Semester II			**16**	
Discipline Specific Elective (DSE) Courses (4 credits)				
Sr. No.	**Course Code**	**Title of the Course**	**Credits**	**Level**
1	ELE-5205	Internet of Things	2T	400
2	ELE-5206	Internet of Things Lab	2P	400
3	ELE-5207	Switching and Routing	2T	400
4	ELE-5208	Switching and Routing Lab	2P	400
Total Credits for DSE Courses in Semester II			**4**	
Total Credits in Semester II			**20**	

Blooms Taxonomy Cognitive Levels	
Cognitive Level	**Notations**
K1	Remembering
K2	Understanding
K3	Applying
K4	Analyzing
K5	Evaluating
K6	Create

BRIDGE COURSE

Title of the Course	Introduction to Electronics
Course Code	ELE-1000
Number of Credits	2
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	Yes
Bridge Course/ Value added Course	Yes
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Introduce fundamental passive components used in electrical and electronic circuits. • Provide a fundamental understanding of semiconductor devices and applications in basic electronic circuits. • Getting familiar with IC's and building different applications using IC's. • To introduce the foundation of communication techniques.	
Course Outcomes:		**Mapped to PSO**
	CO 1. Identify and classify different passive components like resistors, capacitors, and inductors.	PSO 1

	CO 2. Identify and distinguish between active components (Diode, BJT, FET)		PSO 1	
	CO 3. Understanding of OP-AMP, 555 timers, Regulated IC's and Fabrication of integrated circuits.		PSO 1	
	CO 4. To understand and apply the basic analog communication techniques		PSO 1	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	Introduction to active and Passive Components: Definition and role in circuits. Resistors: Basics of resistors, types, tolerance, color coding, power rating, series and parallel connections Capacitors: Basics of capacitors, types, Capacitance, tolerance, voltage rating, charging and discharging behavior, series and parallel connections Inductors: Basic concepts of inductance, types, Mutual coupled coils Semiconductor Diode: P-N junction diode, diode characteristics, Zener & avalanche breakdown Diode as rectifier. Bipolar Junction Transistor (BJT): PNP and NPN transistor, CB, CE and CC configurations. Field Effect Transistor (FET): Construction, operation, characteristics and Biasing of Junction FET.	**15**	CO1, CO2	K1, K2, K3
Module 2:	OP-AMP: Block diagram of OP-AMP, Differential Amplifier configurations, Differential amplifier analysis, characteristics of OP-AMP, applications of OP-AMP. TIMERS: NE 555 timer, working principles, 555 timers as Astable, Monostable and voltage controlled oscillator, and PLL. Regulated IC: 78 & 79 series, IC723, LM317, Line regulation, Load regulation Fabrication of IC's: Advantages of IC's, Epitaxial process, Fabrication of monolithic	**15**	CO3, CO4	K1, K2, K3

	components: NPN and PNP transistors, diodes, resistors and capacitors. Introduction to communication: Block of communication system, Necessity of modulation, Electromagnetic communication spectrum. Amplitude Modulation, Frequency Modulation (FM) and Phase Modulation (PM), modulation index and frequency spectrum.			
Pedagogy:	Lectures/Experiential Learning/Presentations			
Texts:	1. A. K. Sawhney, 'A Course in Electrical and Electronic Measurements and Instrumentation', Dhanpat Rai & Co, 19th Edition, 2020 2. N. N. Bhargava, D. C. Kulshreshtha, S. C. Gupta, 'Basic Electronics and Linear Circuits', Tata MacGraw Hill, 2nd Edition, 2017 3. Ramakant Gayakwad, 'Op-Amps and Linear Integrated Circuits', 4th Edition, Prentice Hall, 2015. 4. George Keneddy,'Electronics Communication Systems', McGraw Hill Education; 5th edition, 2011			
References/ Readings:	1. S. Salivahan, N. Suresh Kumar, 'Electronics Devices and Circuits', 3th Edition, McGraw Hill Education , 2017. 2. Jacob Millman, Christos Halkias, Chetan Parikh, 'Integrated Electronics - Analog And Digital Circuits And Systems, 2ndEdition, 2018 3. Robert F. Coughlin, Frederick F. Driscoll, 'Operational Amplifiers and Linear Integrated Circuits, 5th Edition, Pearson, 1997 4. D Roy Choudhury, Shail B Jain,'Linear Integrated Circuits', 6th Edition, New Age International Private Limited, 2021 5. Simon Haykin, Michael Moher,'Communication Systems', 4th Edition, Wiley, 2006			

SEMESTER I

Discipline Specific Core Courses

Title of the Course	Micro Electronics and VLSI Design
Course Code	ELE-5000
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Introduce to the VLSI Technology, various fabrications processes involved in IC design , • Analysis of Electronics circuits, Design examples of VLSI circuits, Circuit Optimization techniques • Advance circuits designs: Memory, Registers, Synchronous circuits etc.	
Course Outcomes:		**Mapped to PSO**
	CO 1. Understanding design of fundamental gates and customize them for specific electrical and electronics application,	PSO 1

	CO 2. Understand the fabrications processes involved in VLSI technology,		PSO 5	
	CO 3. Apply, Analyze and evaluate the synchronization of combinational and sequential circuits, memory cell and memory array circuits.		PSO 2	
	CO 4. Evaluating Advanced digital circuits and Programmable logics		PSO 2	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	An overview of VLSI, Modern CMOS Technology Silicon Logic, Logic design with MOSFET.	**15**	CO1, CO2	K1, K2
Module 2:	Physical structure of CMOS Integrated circuits Fabrication Technologies of CMOS Integrated Circuits Elements of Physical Design	**15**	CO1, CO2, CO3	K1, K2, K3
Module 3:	Electrical characteristics of MOSFETS Electronic analysis of CMOS Logic gates	**15**	CO3	K4
Module 4:	Advanced Techniques in CMOS Logic Circuits System specifications using HDL, General VLSI components Memories and Programmable Logic	**15**	CO3, CO4	K5
Pedagogy:	Lectures/Experiential Learning			
Texts:	Introduction to VLSI Circuits and Systems, John P. Uyemura, WILLEY.			
References/ Readings:	1. Principles of CMOS VLSI Design, N.H.E. W. &Eshahiraghian, Addison Wesley 2. Modern VLSI Design System on Silicon, Pearson Education Asia. By W. Wolf. 3. VLSI Technology, S.M. Sze, McGraw -Hill (1995). 5.Basic VLSI Design, Douglas Pucknell, K. Eshraghian, Prentice Hall India.			
Web Resources:	https://www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-itrs/			

Title of the Course	Signals and Systems
Course Code	ELE-5001
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to • Introduce the fundamentals of signals and systems, including signal characterization and basic processing operations. • Develop an understanding of discrete-time signals and systems, and the methods of analysing them. • Provide a comprehensive understanding of the Fourier, Laplace, and other transforms used in signal analysis. • Explore digital filter structures and design techniques for FIR and IIR filters.	
Course Outcomes:		**Mapped to PSO**
	CO 1. Classify and analyse different types of signals and understand basic signal processing operations and DSP practical applications.	PSO 3
	CO 2. Apply mathematical models to describe discrete-time signals and systems, including	PSO 3

	sampling and correlation.			
	CO 3. Compute and interpret various transforms (Fourier, Laplace, Wavelet, STFT) for signal analysis.		PSO 3	
	CO 4. Design and analse FIR and IIR digital filter structures		PSO 3	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	1.1 Characterization and Classification of Signals, Typical Signal Processing Operations	**06**	CO1	K1, K2
	1.2 Discrete-Time Signals, Sequence Representation, Sampling Process, Simple Interconnection Schemes, Convolution, Correlation of Signals	**09**	CO2	K2
Module 2:	2.1 Fourier series, Continuous and Discrete-time Fourier Transform, Laplace Transform,	**07**	CO2, CO3	K1, K2. K3
	2.2 Energy Density Spectrum, Phase and Group Delays	**04**	CO3	K1, K2
	2.3 Short-Time Fourier Transform, Wavelet Transform	**04**	CO2, CO3	K1, K2. K3
Module 3:	3.1 Digital Processing of Continuous Time Signals - Sampling of Continuous Time Signal, Low-pass & Band-pass Signal, Anti-Aliasing, Sample-and-Hold (S/H)	**04**	CO2, CO3	K2
	3.2 Digital Filter Structure - Block Diagram Representation, FIR, IIR filter, Allpass Filter, Tunable IIR Digital Filter, Digital Sin-Cosine Generator.	**07**	CO2, CO3	K4, K5
	3.3 FIR Digital Filter Design - Preliminary Considerations, FIR Filter Design Based on Windowed Fourier Series	**04**	CO2, CO3	K4, K5
Module 4:	4.1 DSP Algorithm Implementation - Computability Equation Describing Filter Structure, Verification, Number Representation, Handling Overflow	**07**	CO1	K4, K5
	4.2 Dual-Tone Multi-Frequency Signal Detection, Musical Sound Processing,	**08**	CO1	K4

	Signal Compression, Transmultiplexers			
Pedagogy:	Lectures/Experiential Learning			
Texts:	Sanjit K Mitra, 'Digital Signal Processing: A computer Based Approach, 3rd Edition, Tata MacGraw-Hill, 2011			
References/ Readings:	1. Johnny R. Johnson, Introduction To Digital Signal Processing, Prentice Hall, 1989. 2. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing, 4th Edition, Pearson Education, 2007. 3. Simon Haykin, Van Veen, Signals and Systems, 2nd Edition, Wiley, 2007 4. Richard G. Lyons, 'Understanding Digital Signal Processing', Pearson, 2022 5. S. Palani, 'Signals and Systems', Springer International Publishing, 2021			

Title of the Course	Embedded System Design
Course Code	ELE-5002
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	NIL	
Course Objectives:	This course is intended to: • Introduce with Architectures of Microcontroller and its programming with Interfacing various Interfaces is discussed in depth in this paper. • Programming in assembly as well as in C for 8/16/32 bit controller • Implementation of embedded system projects	
Course Outcomes:		**Mapped to PSO**
	CO 1. Understand the architecture and programming of microcontrollers and embedded processors.	PSO 1
	CO 2. Apply knowledge of embedded system hardware components such as sensors, actuators, memory, and communication interfaces.	PSO 1

	CO 3. Develop embedded C programs for microcontrollers (e.g., 8051, PIC, ARM) to perform real-time tasks.		PSO 5	
	CO 4. Design and simulate embedded systems for real-time applications using suitable development tools and environments.		PSO2, PSO 5	
	CO 5. Integrate hardware and software to create a working embedded solution for given specifications.		PSO5	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: Introduction to Controller	Computer Architecture, RISC/CISC and Princeton Architectures	**5**	CO1	K1, K2
Module 2: Embedded system	Definition, Basic Block, Designing of System, Applications	**5**	CO1	K1, K2, K3
Module 3: 8-bit Micro controller	3.1 Introduction to various 8-Bit microcontroller, 8051 features, Architecture	**3**	CO1	K1, K2
	3.2 Memory organization, Instruction set	**4**	CO1	K2, K3
	3.3 Interrupts, Timer/counter, LED, Switches, ADC, DAC, LCD Interfacing,	**4**	CO2	K2, K3
	3.4 Programming in Assembly and C	**4**	CO3	K3, K4, K5
	3.4 Implementation of embedded project using 8051	**4**	CO4, CO5	K2, K3, K6
Module 4: 16-bit Micro controllers	4.1 PIC controller Introduction, Architecture	**2**	CO1	K1, K2
	4.2 Instruction set	**4**	CO1	K2
	4.3 Peripheral interfaces: LED, LCD, Serial RS232	**3**	CO2	K3
	4.4 Programming in C	**2**	CO3	K3, K4, K5
	Implementation of embedded project using PIC	**4**	CO4, CO5	K2, K3, K6

Module 5: 32-bit Micro controllers	5.1 ARM Introduction, ARM architecture	**2**	CO1	K2
	5.2 ARM Exception Handling, Timers/Counters	**2**	CO1	K1, K2
	5.3 UART, SPI, PWM, WDT, Input Capture, Output Compare Modes, I2C	**3**	CO2	K2
	THUMB/ARM instruction	**2**	CO1	K2
	Programming in C.	**2**	CO3	K3, K4, K5
	Implementation of embedded project using 8051	**4**	CO4, CO5	K2, K3, K6
Pedagogy:	Lectures/Experiential Learning			
Texts:	1. Lipovski G. J. Single and multiple Chip Microcontroller interfacing. Prentice Hall, USA 1998. 2. Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay "The 8051 Microcontroller and Embedded Systems: Using Assembly and C", 2nd Edition (2007), Pearson.			
References/ Readings:	Jan Holler, VlasiosTsiatsis, Catherine Mulligan, StefanAvesand,StamatisKarnouskos, David Boyle, "From Machine-to-Machine to theInternet of Things: Introduction to a New Age of Intelligence", 1st Edition, Academic Press, 2014.			

Title of the Course	Electronics Practicals -I
Course Code	ELE-5003
Number of Credits	04
Theory/Practical	Practicals
Level	400
Effective from AY	2025-2026
New Course	Yes
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Give the hands-on experience to design the basic digital and analog circuits • Simulate the various digital modulation techniques and data correction and detection used in general communication system. • Expose students to design digital circuits using microwind. • Implement numerical algorithm. • To provide practical knowledge of implementing digital signal processing techniques such as filtering, aliasing, interpolation, DFT, and FFT algorithms. • Design and implement system models using transfer functions and convolution operations for signal analysis and transformation.	
Course Outcomes:		**Mapped to PSO**

	CO 1. learn the basics of a communication system for modulation, data coding, error coding channel coding methods.		PSO 1	
	CO 2. Design signal conditioning and VLSI circuits for various applications.		PSO 2	
	CO 3. Apply, Analyse and evaluate the synchronization of combinational and sequential circuits, memory cell and memory array circuits.		PSO 3	
	CO 4. Implement and analyze digital filters, demonstrate the effects of aliasing, and interpolation		PSO 3	
	CO 5. Develop and implement DFT, FFT, and convolution-based systems to perform frequency-domain and time-domain analysis.		PSO 3	
	CO 6. Design applications using Various embedded platforms			
Content:	Note: Minimum 4 experiments are to be performed from Each Module	**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	1. Design of counters for digital clock (using Microwind s/w) 2. Multiplexer and Demultiplexer (using Microwind s/w) 3. Encoder and Decoder (using Microwind s/w) 4. 2nd order Butter-worth Notch Filter (p-Spice) 5. Buffer design using SPICE (p-Spice) 6. Memory design using 6T cell	**40**	CO1, CO2, CO3	K4, K5, K6
Module 2:	1. Implementation of Filters – Ensemble Average filter, Exponential weighted running system, Median Filter. 2. Implementation of the aliasing effect 3. Implementation of interpolation 4. Implementation of DFT and FFT algorithms 5. Design Transfer function and convolution	**40**	CO1	K3, K4, K6
Module 3:	1. Design of variable Power Supply for 2Amp with Load and Line regulation. 2. Design of Function generator 3. Design of Stepper drive with monoshot	**40**	CO 6	K2, K3, K4, K6

	4. Serial Transmission and reception PIC16F877 5. Data acquisition with ADC PIC16F877 on microcontroller 6. Hex Keypad Interfaced to ARM controller & display on LCD			
Pedagogy:	Presentations /assignments/Experiential learning			
Texts:	1. Introduction to VLSI Circuits and Systems, John P. Uyemura, WILLEY. 2. Sanjit K Mitra, 'Digital Signal Processing: A computer Based Approach, 3rd Edition, Tata MacGraw-Hill, 2011 3. Lipovski G. J. Single and multiple Chip Microcontroller interfacing. Prentice Hall, USA 1998.			
References/ Readings:	1. Principles of CMOS VLSI Design, N.H.E. W. &Eshahiraghian, Addison Wesley 2. Basic VLSI Design, Douglas Pucknell, K. Eshraghian, Prentice Hall India. 3. Johnny R. Johnson, Introduction To Digital Signal Processing, Prentice Hall, 1989. 4. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing, 4th Edition, Pearson Education, 2007. 5. Simon Haykin, Van Veen, Signals and Systems, 2nd Edition, Wiley, 200 6. Richard G. Lyons, 'Understanding Digital Signal Processing', Pearson, 2022 7. S. Palani, 'Signals and Systems', Springer International Publishing, 2021 8. Jivan Parab etal., Exploring C for microcontroller (Springer 2007)			
Web Resources:	https://www.cadence.com			

Discipline Specific Elective Courses

Title of the Course	EDA Tools
Course Code	ELE-5201
Number of Credits	02 (2T)
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Familiarize the students with industry-oriented EDA tools. • Each Quartus, ISE compilations and programming and its use for design and analysis. • Enable the student to extract various design parameters from simulation results.	
Course Outcomes:	The students will,	**Mapped to PSO**
	CO 1. Understand the EDA workflow for ASIC and FPGA design.	PSO 1
	CO 2. Learn to model digital systems using HDL (VHDL).	PSO 2
	CO 3. Analyse logic using Chip scope	PSO 4

	CO 4. Perform simulation, synthesis, place & route, and timing analysis		PSO2	
	CO 5. Use EDA tools such as Xilinx Altera wave Analysis ,Modelsim tools.		PSO 1	
	CO 6. Gain experience in RTL design and testbench development.		PSO 2	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: EDA and HDL basics	1.1 Introduction to EDA & VLSI Design Flow	**3**	CO1	K1
	1.2 HDL coding basics	**8**	CO2	K2
	1.3 HDL Modeling Styles: Dataflow, Behavioural, Structural	**2**	CO2	K2
Module 2: EDA Tools	2.1 Introduction to lab tools and environment setup	**7**	CO5	K2
	2.2 Introduction Quartus and ISE webpack, Model sim, Chip scope	**10**	CO3	K2, K3
Pedagogy:	Lectures/Experiential Learning/Presentations			
Texts:	1. Design through Verilog HDL By T. R. Padmanabhan & Sundari. IEEE press, Wiley Interscience. 2. Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon) 26 March 2009 3. Hands on experience on alteradevelopment board byJ.S.Parab,etal: Springer Netherland. 2018(ISBN 978-81-322-3769-3)			
References/ Readings:	http://www.xilinx.com/itp/xilinx7/help/iseguide/html/ise _fpga_design_flow_overview.htm			

Title of the Course	EDA Tools I
Course Code	ELE-5202
Number of Credits	02 (2P)
Theory/Practical	Practical
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	NIL	
Course Objectives:	This course is intended to: • Familiarize the students with industry-oriented EDA tools. • Each Quartus, ISE compilations and programming and its use for design and analysis. • Enable the student to extract various design parameters from simulation results.	
Course Outcomes:	The students will be experiential hand-on on following.	**Mapped to PSO**
	CO 1. Understand the EDA workflow for ASIC and FPGA design.	PSO 1
	CO 2. Learn to model digital systems using HDL (VHDL).	PSO 2
	CO 3. Analyse logic using Chip scope	PSO 4
	CO 4. Perform simulation, synthesis, place & route, and timing analysis	PSO2

	CO 5. Use EDA tools such as Xilinx Altera wave Analysis ,Modelsim tools.		PSO 1	
	CO 6. Gain experience in RTL design and testbench development.		PSO 2	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: **Practical**	1.1 Study of Phases of Quartus compilations. 1.2 Study of phases of ISE compilations 1.3 Testing logic using ChipScope-I. 1.4 Testing logic using ChipScope-II 1.5 FIFO implementation 1.6 Pulse stretcher 1.7 Test bench using Modelsim-I 1.8 Test bench using Modelsim-I	**60**	CO3, CO6	K2, K3, K4, K5, K6
Pedagogy:	Lectures/Experiential Learning/Presentations /laboratory design and implementation			
Texts:	1. Design through Verilog HDL By T. R. Padmanabhan & Sundari. IEEE press, Wiley Interscience. 2. Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon) 26 March 2009 3. Hands on experience on alter a development board by J.S.Parab,etal: Springer Netherland. 2018(ISBN 978-81-322-3769-3)			
References/ Readings:	http://www.xilinx.com/itp/xilinx7/help/iseguide/html/ise_fpga_design_flow_overview.htm			

Title of the Course	Numerical Computation and Algorithms
Course Code	ELE-5203
Number of Credits	02 (2T)
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Students should have a knowledge of computer programming	
Course Objectives:	The course is intended to • Develop the basic understanding of numerical computation and algorithm. • Develop skills to implement algorithms to solve mathematical problems on the computer. • To provide basic knowledge of data structure.	
Course Outcomes:	Students will be	**Mapped to PSO**
	CO 1. Student will understand basics of programming language	PSO4
	CO 2. The students will use data structures like Lists, Stack, Queue, and Binary Trees.	PSO4
	CO 3. The students will solve a linear system of equations using an appropriate numerical method.	PSO4

	CO 4. The students will use numerical methods for solving a problem, locate and use good mathematical software to achieve the required accuracy for a particular application, get the accuracy you need from the computer, assess the reliability of the numerical results.		PSO4	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: Computer Programming	Introduction to Algorithms, Elements of Computer Programming language, Basics of algorithm design, general model.	**6**	CO1	K1, K2
Module 2: Data Structures	Introduction to Data Structures, Vectors and Lists, Stack, Queue, Binary Trees.	**6**	CO2	K1, K2
Module 3: Theory of Numerical programming	Numerical Integration: Theory of numerical errors, Trapezoidal & Simpsons rule, Romberg method, Improper integrals. Numerical Solution of linear equations: Gauss-Jordon elimination. Numerical Solutions of nonlinear equations: Bracketing, bisection, Secant, Regula falsi& Newton Raphson method. Numerical Solutions to Ordinary differential equations: Runge-Kutta method, Modified midpoint method.	**18**	CO3, CO4	K2, K3, K5
Pedagogy:	Lectures/Experiential Learning			
Texts:	1. Data structures using C and C++ by Yedidyah Langsam, Moshe J Augenstein, Aaron M Tenenbaum, Prentice Hall of India, 1995 2. Numerical Recipes in C, William H. Press, Brain P. Flannery, William T. Vetterling, Saul A.Teulosky, Cambridge University Press,1990.			
References/ Readings:	1. Data Abstraction and Problem solving in Java by Frank M Carrano, Janet J Prichard ,Addison-Wesley,2001. 2. Numerical Mathematical Analysis, J. B. Scarborough, Oxford and IBM Publishing Company (1979). 3. Numerical Recipes in C: The Art of Scientific Computing by William H Press, Brian P Flannery, Saul A Teukolsky - Mathematics – 1992.			

Title of the Course	Numerical Computation and Algorithms Lab
Course Code	ELE-5204
Number of Credits	02 (2P)
Theory/Practical	Practical
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Students should have a knowledge of computer programming	
Course Objectives:	The course is intended to • Develop the basic understanding of numerical computation and algorithm. • Develop skills to implement algorithms to solve mathematical problems on the computer. • To provide basic knowledge of data structure.	
Course Outcomes:	Students will be given hand-on with the following topics	**Mapped to PSO**
	CO 1. Student will understand basics of programming language	PSO4
	CO 2. The students will use data structures like Lists, Stack, Queue, and Binary Trees.	PSO4
	CO 3. The students will solve a linear system of equations using an appropriate numerical method.	PSO4

	CO 4. The students will use numerical methods for solving a problem, locate and use good mathematical software to achieve the required accuracy for a particular application, get the accuracy you need from the computer, assess the reliability of the numerical results.		PSO4	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: Practicals	1. Push and pop operation on stack 2. Insert and delete operation on queue 3. Insertion and deletion operation on linked list 4. Traversing a binary tree 5. Read two 3X3 matrix, add them and display their sum 6. Numerical Programming 1 (Trapezoid method) 7. Numerical Programming 2 (Simposons 1/3 method) 8. Numerical Programming 2 (Bisection method) 9. Numerical Programming 6 (Gauss-Jordon elimination method) 10. Numerical Programming 3 (RungeKutta method) 11. Numerical Programming 4 (Newton Raphson method) 12. Numerical Programming 5 (Regula Falsi method) 13. Numerical Programming 6 (Secant method)	**60**	CO1, CO4	K2, K5
Pedagogy:	Experiential Learning			
Texts:	1. Data structures using C and C++ by Yedidyah Langsam, Moshe J Augenstein, Aaron M Tenenbaum, Prentice Hall of India, 1995 2. Numerical Recipes in C, William H. Press, Brain P. Flannery, William T. Vetterling, Saul A.Teulosky, Cambridge University Press,1990.			
References/ Readings:	1. Data Abstraction and Problem solving in Java by Frank M Carrano, Janet J Prichard ,Addison-Wesley,2001. 2. Numerical Mathematical Analysis, J. B. Scarborough, Oxford and IBM Publishing Company (1979). 3. Numerical Recipes in C: The Art of Scientific Computing by William H Press, Brian P Flannery, Saul A Teukolsky - Mathematics – 1992.			

SEMESTER II

Discipline Specific Core Courses

Title of the Course	Advanced Digital Communication Systems
Course Code	ELE-5004
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	NIL	
Course Objectives:	This course is intended to: • Introduce to students with basics of wireless systems – concepts, theory. • Covers various modulation techniques, to enable the student to synthesize and • Analyse wireless and mobile cellular communication systems over a stochastic fading channel • Mitigation and diversity techniques	
Course Outcomes:	Students will be	**Mapped to PSO**
	CO 1. understand the design, specifications and the performances of various wireless	PSO 1

	communication systems.			
	CO 2. Apply the cellular concepts to evaluate the signal reception performance in a cellular network.		PSO 4	
	CO 3. Apply the traffic analysis to design cellular network with given quality of service constraints.		PSO 3	
	CO 4. Determine the appropriate model of wireless fading channel based on the system parameters and the property of the wireless medium.		PSO 2	
	CO 5. Analyze and design receiver and transmitter diversity techniques.		PSO2, PSO 4	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: Introduction to Mobile and Cellular Communication Systems:	Definitions, impact of Mobile and Cellular Radio Communication Historical overview. Fundamental of Radio Mobile and Cellular Practices Radio mobile links and cells, Frequency re-use, Principles of Cellular Com. Mobile Telephone Switching Subsystem, The mobile frequency spectrum, Hand-off, Cochannel and adjacent channel interference limitations, Near-far problem, Power Control.	**5**	CO1, CO2	K1, K2
Module 2: Mobile Communication Channel including antennas	The mobile wireless propagation channel, Notions on antennas especially the near and far field concept, Line of Sight (LOS) propagation, Multipath fading , outdoor and Indoor Propagation, Flat and selective fading, Special antennas for base stations and headsets, Deterministic, Empirical and Statistical Methods for propagation link computations.	**10**	CO1, CO3, CO4	K2, K3
Module 3: Overview of Mobile and Cellular Radio Communication Modulation and Detection Techniques:	Analog modulations and detection: AM, FM, PM, ACSB, Hybrid and Digital modulation: PCM, ASK, FSK, QPSK, QAM, MSK, etc, Coherent and noncoherent detection, C/N, S/N, Eb/No and BER relations, Probability concepts, Mobile Radio links parameters.	**15**	CO1, CO2, CO4	K3, K4

Module 4: Overview of Multiple Accesses Techniques	Simplex, Duplex TDD and Time Division Duplex, Time division multiple access (TDMA) FDMA and OFDM, Code Division multiple access (CDMA), Hybrid multiple access, Management of voice, Data and Video (Multimedia) information.	**12**	CO1	K2
Module 5: Modern Digital Radio Systems	standards, proposals and comparisons GSM (Europe and all over the world) - TDMA, IS-54 (U.S.A.)- TDMA, IS-95 (U.S.A., Korea) CDMA-, PHS (Japan) - TDMA, Frequency Hopping (FH) (U.S.A.) - CDMA, PCS, PCS Cordless telephone 2nd generation (CT-2), Cellular digital packet data (CDPD), and Wireless LAN, New standard trends Edge, 3rd and 4th generation beginning, LTE	**10**	CO3, CO4	K2, K3, K4
Module 6: Mitigation Techniques for Mobile System	Overview of Natural and manmade external noise sources, Radiation hazards effects from base stations, Mobile and portable equipments.	**04**	CO1	K1, K2
Module 7: Diversity Techniques for Mobile Radio Systems	Dispersive channels, Space diversity, Frequency diversity, Equalizer techniques	**04**	CO4	K2, K3
Pedagogy:	Lectures/Experiential Learning			
Texts:	Rappaport, T.S., "Wireless Communications: Principles And Practice, 2/E,Pearson			
References/ Readings:	1. Steele, R., Hanzo, L., "Mobile Radio Communication" 3rd Edition Wiley 2005. 2. Wireless Communications (WIRELESS COMMUNICATIONS, 2ND ED, Molisch A F),Wiley			

Title of the Course	Real Time Operating Systems
Course Code	ELE-5005
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • To focus on the concept of highlighting the various methods of improvising speed of computing machine through the operating system organization and various entity managements. • To analyse the small embedded system developments through the Real Time Operating Systems for task management efficiency. • Porting RTOS on embedded platform	
Course Outcomes:	The student will:	**Mapped to PSO**
	CO 1. Generalize the understanding of the computing machine and various entities associated with the enhancement of the efficiency.	PSO 1
	CO 2. Handle the operating system management process, memory, I/O, Secondary Disk and	PSO 4

	organizations of various.			
	CO 3. Handle any operating system for process and task management if follows the documentations of the same.		PSO 5	
	CO 4. able to design any real time application using RTOS		PSO 5	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	**Introduction to Computer Organization and Architecture:** hardware vs. software -the virtual machine concept, the concept of von Neumann architecture, hardware components and functions, trends in hardware development, system configurations and classifications. **The Central Processing Unit: CPU** components, register sets, instruction cycles, addressing modes, instruction sets, the concept of micro-programming, Basics of RISC approach, pipelined and super-scalar approaches, vector processors and parallel processors, hardware support for the OS.	**15**	CO1, CO2	K1, K2
Module 2:	**Process Description and Control:**Processes, process states, processor modes, context switching, CPU scheduling algorithms, threads Concurrency Control: Concurrent processes, critical section problem and solutions, mutual exclusion solution requirements, semaphores and monitors.	**15**	CO2, CO3	K2, K3, K4
Module 3:	**Deadlocks:**Characterization, detection and recovery, avoidance, prevention **Inter Process Communication:**classical IPC problems and solutions, IPC techniques. The Memory Subsystem: Memory types and hierarchy, module level Organization, cache memory. Memory partitioning, swapping, paging, segmentation, virtual memory.	**15**	CO1, CO2, CO3	K1, K2 K3 K4
Module 4:	The Input/Output and File Subsystem:I/O devices, controllers and channels, bus structures, 1/0 techniques (programmed, interrupt-driven and DMA), I/O subsystem layers. Concepts of files and directories, issues and techniques for efficient storage and access of data. I/O and file system support for graphics, multimedia, databases,	**15**	CO1, CO2, CO3, CO4	K1, K2, K3, K4, K5, K6

	transaction processing and networking. **µCOS case study**			
Pedagogy:	Lectures/Experiential Learning			
Texts:	Operating system principles, 3rd Edition,by Willian Stallings –PHI(1998)			
References/ Readings:	1. Operating system concepts by Silberchatz and Galvin – Addisionwesley 2. Operating system by Tanaumbuam, PHI New Delhi			

Title of the Course	Digital System Designs
Course Code	ELE-5006
Number of Credits	04
Theory/Practical	Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	Yes

Pre-requisites for the Course:	Should have studied digital electronics at the graduate level	
Course Objectives:	This course is intended to, • Teach principles of combination and sequential logic design • Develop implementation skills using hardware description languages. • Teach and familiarize with industry technologies such as Memory, CPLDS, FPGA.	
Course Outcomes:	Students will be learning theory of following.	**Mapped to PSO**
	CO 1. Understand number system, number system conversion, error detection techniques, Boolean algebra and basic logic gates.	PSO 2
	CO 2. Leverage Hardware description languages for realization of combinational and sequential designs	PSO 2
	CO 3. Understand principles of combination and sequential logic design	PSO 2

	CO 4. Understand the different memories used in computer, programmable logic devices		PSO 2	
	CO 5. Understand the architecture of field programmable gate array, deployment of neural network on FPGA		PSO 3	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1: Introduction	About Digital Design, Analog versus Digital, Electronic Aspects of Digital Design, PLD's, ASIC, Digital Design level. Digital Concept and Number System: General Positional number system conversions, Operation, BCD, Gray Code, Character Codes, Codes for Actions, Conditions, and States nCubes and Distance, Codes for Detecting and Correcting Errors, Error-Detecting Codes, Error-Correcting and Multiple Error-Detecting Codes, Hamming Codes, CRC Codes, Two Dimensional Codes, Checksum Codes, m-out-of-n Codes, Codes for Serial Data Transmission and Storage, Parallel and Serial Data, Serial Line Codes	**6**	CO1	K1, K2
Module 2: Combinational Logic Design Principles and practices	Switching Algebra, Combinational-Circuit Analysis, Combinational-Circuit Synthesis, and Timing Hazards, Documentation Standards, Circuit Timing, Combinational PLDs, Decoders, Encoders, Three-State Devices , Multiplexers, Exclusive-OR Gates and Parity Circuits , Comparators, Adders, Subtractors, and ALUs, Combinational Multipliers, Exclusive-OR Gates and Parity Circuits, Comparators, Adders, Subtractors, and ALUs , Combinational Multipliers.	**8**	CO1, CO3	K2, K3
Module 3: Hardware Description Languages	HDL-Based Digital Design, The VHDL Hardware Description Language, The Verilog Hardware Description Language	**4**	CO2	K2, K3
Module 4: Sequential Logic Design Principles & Practices	Bistable Elements, Latches and Flip-Flops, Clocked Synchronous State-Machine Analysis, Clocked Synchronous State-Machine Design, Designing State Machines Using State Diagrams, State-Machine Synthesis Using Transition Lists, Another State-Machine Design Example, Decomposing State Machines, Feedback Sequential-Circuit Analysis, Feedback Sequential-Circuit Design, Features, Sequential-Circuit Design with VHDL, Sequential- Circuit Design with Verilog, Sequential-Circuit Documentation Standards, Latches and Flip-Flops, Sequential PLDs, Counters, Shift	**12**	C03	K2, K3, K4

	Registers, Iterative versus Sequential Circuits, Synchronous Design Methodology, Impediments to Synchronous Design ,Synchronizer Failure and Metastability			
Module 5: Memory, CPLDS	Read-Only Memory, Read/Write Memory, Static RAM, Dynamic RAM, Complex Programmable Logic Device	**10**	C04	K1, K2
Module 6: Field Programmable Gate Array	Introduction, FPGA Architectures, Configuration: SRAM-Based FPGAs and Antifuse Permanently Programmed FPGAs, Chip I/O, Circuit Design of FPGA Fabrics, Architecture of FPGA Fabrics, FPGA Soft-core Processor Development flow.	**10**	CO5	K2, K3
Module 7: Neural Networks on FPGA	Introduction, Designing a Neuron, Activation functions, Design of layers, Training and validations, Hardware verification, Case study using PYNQ/VITIS AI framework.	**10**	C05	K2, K3, K4
Pedagogy:	Lectures/Experiential Learning			
Texts:	Digital Design Principles and Practices, by John F. Wakerly, Prentice Hall's Fourth Edition.			
References/ Readings:	1. Digital System Design using VHDL: Charles. H.Roth ; PWS (1998) 2. Scott Hauck and Andre DeHon , Reconfigurable Computing, Morgan Kaufmann, 2008 3. SrinivasDevadas, AbhijitGhosh, and Kurt Keutzer, "Logic Synthesis," McGraw-Hill, USA,1994. 4. Neil Weste and K. Eshragian,"Principles of CMOS VLSI Design: A System Perspective,2nd edition, Pearson Education, 2000. 5. Kevin Skahill, "VHDL for Programmable Logic," Pearson Education, 2000. M.N.O. Sadiku,Elements of Electromagnetics 2nd Edition) , Oxford University press, 1995			

Title of the Course	Electronics Practicals-II
Course Code	ELE-5007
Number of Credits	04
Theory/Practical	Practical
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	Nil

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Simulate the various digital modulation techniques and data correction and detection used in general communication systems. • Expose students to design digital circuits using HDL. • Cover experiments using LabVIEW with MyRIO and NI ELVIS Platform • Cover experiments using real time operating systems	
Course Outcomes:	Students will be learning theory of following.	**Mapped to PSO**
	CO 1. Designs application using embedded system using tasks for real time applications.	PSO2
	CO 2. Handle any computing machine using shell script for computing and management.	PSO2

	CO 3. Develop and design some applications based on SPEEDY 33 using LABView, NI ELVIS ,MYRio, Altera DE2 Board.		PSO5	
	CO 4. Develop an android app.		PSO5	
	CO 5. Design, simulate and debug digital circuits using HDL			
	CO 6. Implementation of the communication system for modulation, data coding, error coding channel coding methods.		PSO1, PSO2, PSO4	
Content:	**Note:** Minimum 4 experiments are to be performed from Each Module	**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	1. ASK, FSK modulation & demodulation. 2. Implementation of MSK modulation and demodulation. 3. QPSK, modulation & demodulationDS-CDMA simulation. 4. Channel Coding methods. a. Convolution b. Block code 5. Error detection and correction Algorithm with CRC 6. Error detection and correction Algorithm with Hamming code	**40**	CO1	K2, K2, K4
Module 2:	1. Switching of LED using µ - COS 2. Switching of LED using RTX 3. Switching of LED using FPGA 4. KEY pad and ADC interfacing using RTOS 5. Shell programming – Web Application. 6. Shell programming – System Management	**40**	CO2, CO3	K2, K3, K4, K6
Module 3:	1. VHDL implementation for the Multiplexer & Demultiplexer 2. VHDL Implementation for Encoder & Decoder 3. VHDL implementation for the Counter. 4. LCD and 7 -segment Interfacing using DE2 board 5. UART Interface using DE2 board 6. Echo & Reverberation implementation on speedy33 kit(lab view)	**40**	CO5	K3, K4, K5
Pedagogy:	Lectures/Experiential Learning			

Texts:	Digital Design Principles and Practices, by John F. Wakerly, Prentice Hall's Fourth Edition.
References/ Readings:	1. Lipovski G. J. Single and multiple Chip Microcontroller interfacing. Prentice Hall, USA 1998. 2. Learning Android Game Programming: A Hands-On Guide to Building Your First Android Game 1st Edition

Discipline Specific Elective Courses

Title of the Course	Internet of Things (IOT)
Course Code	ELE-5205
Number of Credits	02
Theory/Practical	2 Theory
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Identify and define the fundamental concepts, terminologies, basic building blocks, characteristics, and applications of IOT. • Understand the IOT protocols, cloud integration, and data communication methods • Demonstrate the integration of sensors, actuators, and embedded technologies for IOT applications. • Analyze and compare various network and communication technologies used in IOT. • Design and develop IOT application for real-world problems.	
Course Outcomes:	Students will be learning theory of following.	**Mapped to PSO**
	CO 1. Define key concept, components, and basic building blocks of IOT.	PSO 1

	CO 2. Explain communication protocols and cloud integration in IOT systems.		PSO 1	
	CO 3. Implement basic IOT applications using embedded controllers, actuators, and sensors.		PSO 2	
	CO 4. Analyze network protocols for IOT applications.		PSO 4	
	CO 5. Design and build IOT solutions for applications like smart agriculture, smart irrigation.		PSO 5	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	1.1 Introduction to IOT – Architecture, Applications of IOT in healthcare, industry, agriculture, and smart cities	**04**	CO1	K1, K2
	1.2 Embedded Systems and IOT Hardware – Overview of advanced ESP32, Raspberry Pi, and Arduino	**06**	CO1	K2
	1.3 Sensing, actuation, and interfacing	**05**	CO1	K1, K2
Module 2:	2.1 IOT Protocols and Communication - Connectivity Protocol (6loWPAN, RFID), Data Protocol (MQTT, CoAP), Communication Protocols (IEEE 802.15.4, Zigbee, Bluetooth, Z-wave).	**07**	CO2	K1, K2
	2.2 Sensing Network - Wireless Sensor Network, Sensor nodes, Node behavior, Stationary and Mobile Wireless Sensor Network.	**04**	CO2	K1, K2
	2.3 Cloud and Fog Computing – Overview of cloud service model, and Fog Computing	**04**	CO2	K2
Pedagogy:	Lectures/Experiential Learning/Presentations			
Texts:	S. Misra, A. Mukherjee, and A. Roy, 'Introduction to IoT', Cambridge University Press, Edition First, 2021			
References/ Readings:	1. S. Misra, C. Roy, and A. Mukherjee, 'Introduction to Industrial Internet of Things and Industry 4.0', CRC Press. 2. Pethuru Raj and Anupama C. Raman, 'The Internet of Things: Enabling Technologies', Platforms, and Use Cases", CRC Press. 3. Arshdeep Bahga and Vijay Madisetti, 'Internet of Things: A Hands-on Approach', Universities Press			

Title of the Course	Internet of Things (IOT) Lab
Course Code	ELE-5206
Number of Credits	02
Theory/Practical	2 Practical
Level	400
Effective from AY	2025-2026
New Course	No
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	Nil	
Course Objectives:	This course is intended to: • Identify and define the fundamental concepts, terminologies, basic building blocks, characteristics, and applications of IOT. • Understand the IOT protocols, cloud integration, and data communication methods • Demonstrate the integration of sensors, actuators, and embedded technologies for IOT applications. • Analyze and compare various network and communication technologies used in IOT. • Design and develop IOT application for real-world problems.	
Course Outcomes:	Students will be learning practicals of following.	**Mapped to PSO**
	CO 1. Define key concept, components, and basic building blocks of IOT.	PSO 1
	CO 2. Explain communication protocols and cloud integration in IOT systems.	PSO 1

	CO 3. Implement basic IOT applications using embedded controllers, actuators, and sensors.		PSO 2	
	CO 4. Analyze network protocols for IOT applications.		PSO 4	
	CO 5. Design and build IOT solutions for applications like smart agriculture, smart irrigation.		PSO 5	
Content:		**No of hours**	**Mapped to CO**	**Cognitive Level**
Module 1:	Practicals based on IoT Device Interfacing, Communication, and Control (Any six)	**30**	CO3, CO4	K2, K3, K4
	1.1 Sensors (temperature, humidity, light, motion) interfacing with ESP 32 and Raspberry Pi			
	1.2 Actuators (relay, motor, buzzer) interfacing with ESP 32 and Raspberry Pi			
	1.3 Implementing client-server communication			
	1.4 Implementing REST API to fetch sensor data			
	1.5 Implementation of MQTT protocol			
	1.6 Task scheduling with RTOS for IOT			
	1.7 Remote monitoring and visualization of sensor data with platforms like Blynk/ThinkSpeak			
	1.8 Controlling the actuator by mobile app			
Module 2:	Practicals based on Wireless Protocols, Cloud Integration, and Smart Applications (Any Six)	**30**	CO3, CO4, CO5	K2, K3, K4, K5, K6
	2.1 Demonstration of Zigbee Communication Protocol			
	2.2 Send and visualize sensor data on cloud platform			

	2.3 Demonstrate wireless sensor network			
	2.4 Implementation of z-wave protocol			
	2.5 Home automation system			
	2.6 Smart lighting system			
	2.7 Smart Irrigation System			
	2.8 Implementation of Data Analytics for IoT			
Pedagogy:	Experiential Learning/Presentations			
Texts:	S. Misra, A. Mukherjee, and A. Roy, 'Introduction to IoT', Cambridge University Press, Edition First, 2021			
References/ Readings:	1. S. Misra, C. Roy, and A. Mukherjee, 'Introduction to Industrial Internet of Things and Industry 4.0', CRC Press. 2. Pethuru Raj and Anupama C. Raman, 'The Internet of Things: Enabling Technologies', Platforms, and Use Cases", CRC Press. 3. Arshdeep Bahga and Vijay Madisetti, 'Internet of Things: A Hands-on Approach', Universities Press			

Title of the Course	Switching and Routing
Course Code	ELE-5207
Number of Credits	2
Theory/Practical	2T
Level	400
Effective from AY	2025-2026
New Course	Yes
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	NIL	
Course Objectives:	This course is intended to: • Introduce the student to the broader understanding of computer networks • Cover Extensive learning in switching and routing technologies. • Comprehensive understanding in LAN switching environment.	
Course Outcomes:	Students will be learning theory of following	**Mapped to PSO**
	CO 1. Study the different network devices, topologies and protocols.	PSO5
	CO 2. Study of IP addressing and subnetting	PSO5
	CO 3. Gain the knowledge about the Switching and Routing	PSO5
	CO 4. Understand the basic device configuration and troubleshooting.	PSO5

Content:		No of hours	Mapped to CO	Cognitive Level
Module 1:	Layered Architecture: Layered Architecture and protocols, Network Devices: Switches, Routers, NIC, Access Points, Modem. Network types: LAN, PAN, MAN & WAN, Topologies: Mesh Topology, Star Topology, Bus Topology, Ring Topology, Hybrid Topology. Network Addressing: IP addressing & Subnet, Classes of IP Addressing, IPv4/IPv6 address & Subnet	**15**	CO1, CO2	K1 K2
Module 2:	Routing Concepts: IP Routing, Types of Routing,Path Determination, Packet Forwarding, IP Routing Table, Dynamic Routing, Default Static Route Open Shortest Path First Concepts: OSPF Features and Characteristics, OSPF Packets, OSPF Operation Switching and Switches, Overview of VLANs, VLAN Configuration, VLAN Trunks, Dynamic Trunking Protocol, Inter VLAN routing, Spanning Tree Protocol	**15**	CO3, CO4	K1 K2
Pedagogy:	Lectures/Practicals/Experiential Learning/ FLIPPED CLASSROOM			
Texts:	CCNA Routing and Switching – Todd Lammle, 2nd Edition, Sybex Publisher (Wiley Brand), 2016.			
References/ Readings:	1. Andrew S.Tanenbaum, 'Computer Networks', 3rd Edition, Prentice Hall. 2. Data Communications and Networking. Forouzan,5th Edition, McGraw Hill, Reprint-2017. 3. James F. Kurose and Keith W. Ross, 'Computer Networking: A Top-Down Approach, 7th Edition, Pearson Education. 4. D-Link Certified, DCS Switching Training Guide.			
Web Resources:	CISCO NETCAD (ONLINE ACCESS)			

Title of the Course	Switching and Routing Lab
Course Code	ELE-5208
Number of Credits	2
Theory/Practical	2P
Level	400
Effective from AY	2025-2026
New Course	Yes
Bridge Course/ Value added Course	No
Course for advanced learners	No

Pre-requisites for the Course:	NIL	
Course Objectives:	This course is intended to: • Introduce the student to the broader understanding of computer networks • Cover Extensive learning in switching and routing technologies. • Comprehensive understanding in LAN switching environment.	
Course Outcomes:	Students will be learning practicals of following	**Mapped to PSO**
	CO 1. Study the different network devices, topologies and protocols.	PSO5
	CO 2. Study of IP addressing and subnetting	PSO5
	CO 3. Gain the knowledge about the Switching and Routing	PSO5
	CO 4. Understand the basic device configuration and troubleshooting.	PSO5

Content:		No of hours	Mapped to CO	Cognitive Level
Module 1: Practicals	1. Study of Network Devices 2. Router Configuration: Configure Initial Router Settings, Configure Interfaces. 3. Router Configuration: Configure the Default Gateway, Ping and Traceroute. 4. DHCPv4 Configuration 5. DHCPv6 Configuration 6. Configure IP Default Static Routes 7. Open Shortest Path First Configuration 8. VLAN Configuration 9. Inter-VLAN routing Configuration 10. Spanning Tree Protocol Configuration	**60**	CO1, CO2 CO3 CO4,	K3, K4
Pedagogy:	Practicals/Experiential Learning/ FLIPPED CLASSROOM			
Texts:	CCNA Routing and Switching – Todd Lammle, 2nd Edition, Sybex Publisher (Wiley Brand), 2016.			
References/ Readings:	1. Andrew S.Tanenbaum, 'Computer Networks', 3rd Edition, Prentice Hall. 2. Data Communications and Networking. Forouzan,5th Edition, McGraw Hill, Reprint-2017. 3. James F. Kurose and Keith W. Ross, 'Computer Networking: A Top-Down Approach, 7th Edition, Pearson Education. 4. D-Link Certified, DCS Switching Training Guide.			
Web Resources:	CISCO NETCAD (ONLINE ACCESS)			