Goa University
P.O.Goa University, Taleigao Plateau, Goa 403206, India

Syllabus of M.E. Electronics and Telecommunications (MICROELECTRONICS)

Implemented from the Academic Year 2008-2009

- **Scope and Purpose:**

  The Masters Programme in Microelectronics, is a two-year specialized Programme, which aims to produce engineers with the practical experience and research skills to satisfy the requirements of the microelectronics industry. The objective of this programme is to provide a thorough and in-depth study in the field of Microelectronics with hands on experience on VLSI Design, HDL programming, FPGA programming, Signal Processing, and Embedded applications. The core programme is supplemented and further reinforced by a well-chosen set of elective courses.

- **Programme Educational Objectives (PEO)**

  To acquire good scientific and engineering knowledge & skills so as to comprehend, analyze, design and create innovative solutions for real life problems.

  To imbibe professional ethics, develop team spirit and effective communication skills to be successful leaders and managers with holistic approach.

  To embrace and explore evolving technologies with due emphasis on environmental and social issues

  Developing entrepreneurial skills with global perspective.

- **Prerequisites:**

  The candidates are required to possess Bachelor's degree in Electronics and Telecommunication / Electronics/ Electrical/ Electrical and Electronics/ Information Technology/ Computers/ Instrumentation/ Biomedical Instrumentation/ Biomedical Electronics/ Process Control /Industrial Electronics/ Power Electronics or AMIE/ IETE or equivalent from recognized University.

- **Credits:**
  The Programme provides for an aggregate of 152 credits, spanning 12 theory Courses, spread across three Semesters, with each Course carrying a uniform six Credits. The lab work is spread across two Semesters, with each 4 lab Courses each carrying 4 Credits and a total of 16 credits. The Project work is spread across two Semesters and carries a total of 40 credits.

- **Course Distribution:**

  First two Semesters, students are offered five (05) Compulsory theory courses and two (02) Compulsory lab courses, totaling seven (07) in first two Semesters. In the third Semester, students are offered two (02) elective courses. The Dissertation work starts in the third Semester and continues till the end of the fourth Semester.

- **Assessment:**

  A student undergoes continuous assessment as well as a semester end assessment. He/She answers three(03) internal tests out of which the best two are considered in granting the Internal credits of 2 each course. He/She is also required to submit assignments, give presentations and do a mini-project. He/She answers a theory paper of 100 marks and 3 hours duration for each theory course at the end of the Semester for six (06) credits per course and practical exam for two courses in the first two Semester for two(02) credits.

1. Course Structure and Scheme of Evaluation (Semester-wise, along with curriculum details)

Semester 1

Subject Code	Name of the Subjects	Hrs / Week		Evaluation (marks)				Credits		
		Lectures	Practical	Internal	External		Total	T	P	I
					Theory	Practical				
MEM 1.1	Semiconductor Devices	4	0	25	100	0	125	6	-	2
MEM 1.2	VLSI Design concepts	4	0	25	100	0	125	6	-	2
MEM 1.3	Hardware Description Languages	4	0	25	100	0	125	6	-	2
MEM 1.4	VLSI Technology	4	0	25	100	0	125	6	-	2
MEM 1.5	Design of Analog/Mixed Mode VLSI Circuits	4	0	25	100	0	125	6	-	2
MEM 1.6	VLSI Design–LAB	0	4	25	0	100	125	-	2	2
MEM 1.7	Hardware Description Languages- LAB	0	4	25	0	100	125	-	2	2

Semester 2

Subject Code	Name of the Subjects	Hrs / Week		Evaluation (marks)				Credits		
		Lectures	Practical	Internal	External		Total	T	P	I
					Theory	Practical				
MEM 2.1	Advanced Digital Signal Processing	4	0	25	100	0	125	6	-	2
MEM 2.2	ASIC Design and FPGA	4	0	25	100	0	125	6	-	2
MEM 2.3	Memory Design and Testing	4	0	25	100	0	125	6	-	2
MEM 2.4	Embedded Systems	4	0	25	100	0	125	6	-	2
MEM 2.5	Testing and Fault Tolerance	4	0	25	100	0	125	6	-	2
MEM 2.6	Digital Signal Processing and Embedded Systems - LAB	0	4	25	0	100	125	-	2	2
MEM 2.7	Designing with FPGA's – LAB	0	4	25	0	100	125	-	2	2

Semester 3

Subject Code	Name of the Subjects	Hrs / Week		Evaluation (marks)				Credits		
		Lectures	Practical	Internal	External		Total	T	P	I
					Theory	Practical				
MEM 3.1	Elective-1	4	0	25	**100**	**0**	125	6	-	2
MEM 3.2	Elective-II	4	0	25	**100**	**0**	125	6	-	2
MEM 3.3	Thesis Seminar	0	20	50	**0**	**100**	150	-	8	4

List of Electives

Elective 1:

E1 System on Chip (SOC)
E2 Sensor Technology and MEMS
E3 Process and Device Characterization and Measurements

Electives 2:

E4 RF Design
E5 Optical Communication
E6 Design for Reliability
E7: Integrated Optics and Optical Networks

Semester 4

Name of the Subjects	Hrs / Week		Credits	Evaluation (marks)				Credits		
	Lectures	Practical		Internal	External		Total	T	P	I
					Theory	Practical				
Thesis		28		50	0	150	200	-	24	4

SYLLABUS
M.E. IN MICROELECTRONICS

SEMESTER 1

1. SEMICONDUCTOR DEVICES:

- Basics Of Semiconductor Physics: Quantum Mechanical Concepts, Carrier Concentration, Transport Equation Bandgap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources.
- Modeling Bipolar Device Phenomena: Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Change Control Model), Transistor Models: Ebber - Molls and Gummel Port Model, Mextram model. Circuit models for diodes, bipolar transistors
- MOSFET Modeling : Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect. Circuit models for MOS devices
- Passive devices like resistors and capacitors, their non-idealities
- Parameter Measurement: General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Biopolar and MOS Transistors.

Texts / References

- S.M. Sze, "Physics of Semiconductor Devices", Wiley Eastern, 1981.
- Philip E. Allen, Douglas R.Hoberg, " CMOS Analog Circuit Design " Second Edition, Oxford Press-2002 (Unit III).
- E.H. Nicollian and J.K. Brews, "MOS physics and technology", John Wiley, 1982.
- Y. Tsibidis," Mixed Analog digital devices and technology", Mc-Graw Hill.
- Richard S. Muller and Theodore I. Kamins " Device Electronics for Integrated Circuits", John Wiley and Sons.
- Edward S. Yang, "Fundamentals of Semiconductor Devices", Mc-Graw Hill.
- Pail Ric hman, "MOS Field Effect Transistor and Integrated Circuits", John Wiley and Sons.

2.VLSI DESIGN CONCEPTS:

- Introduction To MOS Circuits: MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, The Tri State Inverter, Bipolar Devices.

- Circuit Characterization And Performance Estimation: Introduction, Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, and Reliability.

- CMOS Circuit And Logic Design: CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design.

- Systems Design And Design Method: Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing - Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.

- CMOS Sub System Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Texts / References

- N. Weste and K. Eshranghian, "Principles of CMOS VLSI Design", Addison Wesley, 1998.
- Jacob Backer, Harry W. Li and David E. Boyce, " CMOS Circuit Design, Layout and Simulation ", Prentice Hall of India, 1998.
- L.Glaser and D. Dobberpuhl, "The Design and Analysis of VLSI, Circuits", Addison Wesley 1993.
- C.Mead and L. Conway, "Introduction to VLSI Systems", Addison Wesley, 1979.
- Randel & Geiger, " VLSI Analog and Digital Circuit Design Techniques" McGraw-Hill,1990.
- Sahib H.Gerez, "Algorithms for VLSI design automation ",1998.
- William M. Penny, Lillian Lau, " MOS Integrated Circuits- Theory, Fabrication, Design and System Applications of MOS LSI", Van Nostrand Reihold Company.
- Sung Ms Kang, Yusuf Lablebici, "CMOS Digital Integrated Circuits Analysis & Design", Tata Mc-Graw Hill.

3. HARDWARE DESCRIPTION LANGUAGES:

- Basic concepts of hardware description languages.
- Hierarchy, Concurrency, logic and delay modeling.
- Structural, Data-flow and Behavioral styles of hardware description.
- Architecture of event driven simulators.
- Syntax and Semantics of VHDL.
- Variable and signal types, arrays and attributes.
- Operators, expressions and signal assignments.
- Entities, architecture specification and configurations.
- Component instantiation.
- Concurrent and sequential constructs.
- Use of Procedures and functions,
- Examples of design using VHDL.
- Syntax and Semantics of Verilog.
- Variable types, arrays and tables.
- Operators, expressions and signal assignments.
- Modules, nets and registers,
- Concurrent and sequential constructs.
- Tasks and functions,
- Examples of design using Verilog.
- Synthesis of logic from hardware description.
- Case Study and Mini Project

Texts / References

- Douglas Perry, "VHDL", McGraw Hill International (NY), 1993, The Institute of Electrical and Electronics Engineers.
- Navabi," VHDL Analysis & Modeling of digital systems",1998, McGraw Hill .
- S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall (NJ, USA), 1996.
- J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing, Allentown, PA) 1998.
- Stefan Sjoholm & Lennart Lindth,"VHDL for Designers", Prentice Hall.
- Peter J Ashenden, "The Designer's Guide to VHDL ", Morgan Kaufmann Publishers.
- "IEEE std 1364-95, Verilog Language Reference Manual", IEEE Press (NY, USA), 1995.

4. VLSI TECHNOLOGY:

- Environment for VLSI technology: clean room and safety requirements, Wafer cleaning process and wet chemical etching techniques

- Impurity incorporation: solid-state diffusion modeling and technology, Ion implantation: modeling, technology and damage annealing; Characterization of impurity profiles

- Oxidation: kinetics of silicon dioxide growth for thick, thin and ultra-thin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; high K and low K dielectrics for ULSI.

- Lithographic techniques: Photolithography techniques for VLSI/ULSI; Mask generation.

- Chemical Vapour deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; epitaxial growth of silicon; modeling and technology.

- Metalisation techniques: evaporation and sputtering techniques. Failure mechanisms in metal interconnects; multilevel Metalisation schemes.

- Masking Sequence and Process flow for MOS and BIPOLAR Devices

- Topological Design rules

Text/References

- S.M.Sze (Ed), "VLSI Technology", 2nd Edition, McGraw-Hill, 1988.
- Streetman," VLSI Technology".
- C.Y. Chang and S.M. Sze (Ed), "ULSI Technology", McGraw-Hill Companies Inc., 1996.
- S.K.Gandhi, "VLSI fabrication Principles",John Wiley Inc., New York, 1983.
- Sorab K. Gandhi, "The Theory and Practice of Microelectronics", John Wiley & Sons
- B.G Streetman, "VLSI Technology" , Prentice Hall, 1990.
- A.S Grove, "Physics and Technology of semiconductor devices", John Wiley & Sons, 1967.

5.DESIGN OF ANALOG/ MIXED MODE VLSI CIRCUITS:

- Basic CMOS Circuit Techniques, Continuous Time And Low voltage Signal Processing: Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

- Basic BiCMOS Circuit Techniques, Current -Mode Signal Processing: Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters.

- Sampled-Data Analog Filters, Over Sampled A/D Converters And Analog Integrated Sensors: First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

- Analog VLSI Interconnects: Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

- Statistical Modeling And Simulation, Analog Computer-Aided Design And Analog And Mixed Analog-Digital Layout: Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

Text/References

- Paul R. Gray and Robert G.Meyer, " Analysis and Design of Analog Integrated Circuits", John Wiley & Sons.
- Mohammed Ismail, Terri Fiez, " Analog VLSI signal and Information Processing ", 1994, McGraw-Hill International Editons.
- Behzad Razavi, " Design of Analog CMOS Integrated Circuits", Tata Mc-Graw Hill.
- Y. Tsividis, " Mixed Analog-Digital Devices and Technology", Mc-Graw Hill.
- Alan B. Gnebene, " Bipolar and MOS analog integrated circuit design",John Wiley & Sons.
- Mohammed I. Elmasy," Digital Bipolar circuits ", John Wiley & Sons.
- Greogorian & Tames, " Analog Integrated Circuit For Switched Capacitor Circuit "

6.VLSI DESIGN - LAB

- NMOS Inverter-Depletion and Enhancement Mode Circuit Simulation and Adjustment of Vth VLSI Vm parameters for NMOS inverter.

- CMOS Inverter

Circuit Simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners).
Layout of CMOS Inverter, Extraction of parasitics and back annotation and related modifications in circuit parameters and layout.

- Current Source / Mirror

Circuit simulation of current Mirror using BJT and MOS (Simple, Wilson and Widler configurations) study and modifications to improve power and load regulation.
Layout of CMOS Current Mirror.

- 8 Bit shift register cell

Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

- Differential Amplifier

Study of specifications of Differential amplifier and Design considerations. Study of input loading and biasing techniques.

7.HARDWARE DESCRIPTION LANGUAGE – LAB:

- 2 Bit-Counter-The purpose of this lab is to write a HDL description of 2-bit counter as a finite state machine (FSM). The 2-bit counter has several inputs such as clk, rst, enable, load, ... and should be able to reset, accept an input, count-up or count-down, etc...

- Parallel to Serial Converter-The purpose of this lab is to write a HDL description of a parallel to serial converter as an FSMD. The parallel to serial converter will accept an eight-bit number and send one bit of data over the data line per clock cycle. There is also a go bit, which tells the converter to start transmitting data.

- VHDL Calculator-The purpose of this lab is to implement a finite state machine in VHDL to perform simple calculations like addition, subtraction, and multiplication.

- A Simplified HDL UART -In this lab the students design a UART to send data to the PC.

- I2C Bus Lab -HDL implementation of I2C bus protocol

- Design Of A Hardware Multiplier -In this lab students are going to implement hardware multiplier using Sequential Circuit Components.

- ALU Design-The purpose of this lab is to build a 4/8 -bit ALU. The ALU is written behaviorally. It should take in two numbers and be able to add the numbers, subtract the numbers, NOR the numbers, or NAND the numbers.

SEMESTER 2

1. ADVANCED DIGITAL SIGNAL PROCESSING:

- Review of Fourier Transforms, Z-Transforms, Discrete Fourier Transform, Fast Fourier Transform, Convolution And Correlation.
- Design of digital filters: introduction to filter design, types of digital filters, choosing between, FIR and IIR filters, filter design steps, effect of finite register length in filter design, realization of IIR digital filters and fir digital filter, design of IIR filters from continuous time filters, design of fir filters by windowing.
- Digital signal processors: general and special purpose digital signal processors, computer architecture for signal processing, selecting digital signal processors, architecture and programming of ADSP 2181 processor.
- Spectrum estimation: non-parametric methods correlation method, co-variance estimator, performance analysis of estimators, consistent estimators, AR, MA, ARMA signal modeling parameter estimation using yule-walker method.
- Linear estimation and predication: maximum likelihood criterion efficiency of estimator, least mean squared error criterion, recursive estimators, and linear predications.
- Multirate digital signal processing: Mathematical description of change of sampling rate, interpolation and decimation, continuous time model, direct digital domain approach, interpolation and decimation by an integer factor, single and multistage realization, applications of sub band coding.
- Adaptive Filters: Applications Of Adaptive Filters, Adaptive Direct Form FIR Filters: The LMS Algorithm, Adaptive Lattice Ladder Filters, Recursive Least Squares Lattice Ladder Algorithms.
- Introduction to DSP ASIC Design, Configurable Logic for Digital Signal Processing, Design Methodology for DSP, VLSI Implementation of DSP Processors

Text/References

- Monson H.Hayes, " Statistical Digital Signal Processing and Modeling ", John Wiley and Sons, Inc., New York, 1996
- Emmanuel C.Ifeachor Barrie W.Jervis, “Digital Signal Processing”, Pearson Education Asia
- Proakes Manolakis ,” Digital Signal Processing principles, algorithms, and applications”, Prentice Hall India
- ADSP 2181 manuals
- Keshab K. Parhi, ” VLSI DSP Systems; Design & implementation” , Wiley InterScience Publishers
- John G. Proakis, Charles M. Rader, Fuyun Ling, Chrysostomos L. Nikias, Marc Moonen, Ian k. Proudler, ” Algorithms for statistical signal processing”, Pearson Education Asia

2. ASIC DESIGN AND FPGA:

- Introduction To ASICS, CMOS Logic And ASIC Library Design
  Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture.
- Review of VHDL/Verilog: Entities and architectures
- Programmable Asics, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells
  Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.
- Programmable ASIC Interconnect, Programmable ASIC Design Software And Low Level Design Entry
  Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation.
- ASIC Construction, Floor Planning, Placement And Routing
  System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.
- Design using Xilinx family FPGA

Text/References

- M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997
- Skahill, Kevin," VHDL for Programmable Logic", Addison-Wesley, 1996
- John F. Wakherly, " Digital Design: Principles and Practices", 2nd Edn 1994, Prentice Hall International Edn
- Charles W. Mckay, "Digital Circuits a proportion for microprocessors", Prentice Hall

3.MEMORY DESIGN AND TESTING:

- Random Access Memory Technologies
  Static Random Access Memories (SRAMs):
  SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.
  Dynamic Random Access Memories (DRAMs):
  DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

- Nonvolatile Memories
  Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

- Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance
  RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

- Semiconductor Memory Reliability And Radiation Effects
  General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.
  Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

- Advanced Memory Technologies And High-Density Memory Packaging Technologies
  Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Text/References

- A.K Sharma, " Semiconductor Memories Technology, Testing and Reliability", IEEE Press.
- Luecke Mize Care, " Semiconductor Memory design & application", Mc-Graw Hill.
- Belty Prince, " Semiconductor Memory Design Handbook"
- Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S)

4. EMBEDDED SYSTEMS:

- Introduction And Examples Of Embedded Systems, Concept Of Embedded System Design: Design challenge, Processor technology, IC technology, Design technology, Trade-offs
- Custom single purpose processor hardware, general-purpose processor: introduction, basic architecture, operation, super-scalar and VLSIIW architecture, application specific instruction set processors (ASIPS), microcontrollers, digital signal processors, selecting a microprocessor.
- Memory: Introduction, Memory write ability, Storage performance, Tradeoff s, Common memory types Memory hierarchy and cache
- AVR 8515 microcontroller: Architecture and Programming in assembly and C.
- Interfacing Analog and digital blocks: Analog-to-Digital Converters (ADCs), Digital-to-Analog, Converters (DACs)., Communication basics and basic protocol concepts, Microprocessor interfacing: I/O addressing, Port and Bus based, I/O, Memory mapped I/O, Standard I/O interrupts, Direct memory access, Advanced communication principles parallel, serial and wireless, Serial protocols I2C, Parallel protocols PCI bus, Wireless protocol IrDA, blue tooth.
- Different peripheral devices: Buffers and latches, Crystal, Reset circuit, Chip select logic circuit, timers and counters and watch dog timers, Universal asynchronous receiver, transmitter (UART), Pulse width modulators, LCD controllers, Keypad controllers.
- Design tradeoffs due to thermal considerations and Effects of EMI/ES etc.
- Software aspect of embedded systems: Challenges and issues in embedded software development, Co-design
- Embedded software development environments: Real time operating systems, Kernel architecture: Hardware, Task/process control subsystem, Device drivers, File subsystem, system calls, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin, priority based scheduling, Context switch: Task synchronization: mutex, semaphore, Timers, Types of embedded operating systems, Programming languages: assembly languages, high level languages
- Development for embedded systems: Embedded system development process, Determine the requirements, Design the system architecture, Choose the operating system, Choose the processor, Choose the development platform, Choose the programming language, Coding issues, Code optimization, Efficient input/output, Testing and debugging, Verify the software on the host system, Verify the software on the embedded system

Text /References

- Frankvahid/Tony Givargis, " Embedded System Design- A unified Hardware/software Introduction".
- David E Simon, " An embedded software primer ", Pearson education Asia, 2001.
- Dreamteach Software team," Programming for Embedded Systems"
- AVR 8515 manual
- J.W. Valvano, "Embedded Microcomputor System: Real Time Interfacing"
- Jack Ganssle, "The Art of Designing Embedded Systems", Newnes, 1999.

5. TESTING AND FAULT TOLERANCE:

- Physical Faults and their Modelling
- Stuck-at Faults, Bridging Faults
- Fault Collapsing; Fault Simulation
- Deductive, Parallel, and Concurrent Fault Simulation Critical Path Tracing
- ATPG for Combinational Circuits: D- Algorithm, Boolean Difference, Podem
- Random, Deterministic and Weighted Random Test Pattern Generation Aliasing and its Effect on Fault Coverage
- PLA Testing, Cross Point Fault Model and Test Generation
- Memory Testing - Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests
- Delay Faults; ATPG for Sequential Circuits
- Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board Level Testing
- BIST and Totally Self checking Circuits
- System level Diagnosis; Introduction

- Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes
- Reconfiguration Techniques
- Yield Modelling Reliability and effective area utilization.

Text/References

- Hideo Fujiwara, " Logical testing & design for testability", The MIT Press.
- Mike Tien Chienlee, " High level Test Synthesis of Digital VLSI circuits", Artech House Boston London.
- Viswani D.Agarval Michael L.Bushnell, " Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit ", Kluwer Academic Publications, 1999.

6. DIGITAL SIGNAL PROCESSING AND EMBEDDED SYSTEM LAB:

Digital Signal Processing – LAB

- Accessing Memory-Mapped registers and Non-Memory-Mapped Registers of ADSP 2181 In C
- Programming The ADSP-21xx Timer In C
- FFT implementation using ADSP 2181
- Digital filter design using ADSP 2181.
- Powering up and programming the AD1847 using an ADSP-2100 Family DSP.
- Implementation of adaptive filters using ADSP 2181.

Embedded Systems - LAB

- Decimal Counter and Multiplexing the Output

The purpose of this lab is to implement a decimal counter, which counts from 0 to 99. The students will be required to write a program for the AVR 8515 micro-controller.

- Watchdog Timer

In this lab the students will design a hardware watchdog timer. They are ment to write a buggy program in order to test their WDT. The 8515 program should perform some computation, e.g., write 1, 2, 3 ... to the LED and at some point enter an infinite loop. During normal operation, the 8515 program must periodically (up to 254 second long cycles) write to the WDT's initial value register to avoid unnecessary resets.

- AVR microcontroller UART in C

Implement AVR microcontroller UART in C

- Implementation of simple calculator using AVR 8515

Implement a simple calculator using AVR 8515 microcontroller with keyboard and LCD display interface.

- Analog to Digital Conversion

To be able to implement analog to digital conversion using the ADC0804LCN 8-bit A/D converter. You will design a circuit and program the chip so that when an analog signal is given as input, the equivalent digital voltage is displayed on an LCD display.

- Implementing SPI bus Using AVR 8515

The students are required to implement I2C serial communication using AVR 8515.

- Digital Filters with AVR

Implement digital filters using low cost microcontroller from AVR series.

- Converting 8-bit LCD communication to 4-bit

Interface LCD with AVR 8515 using only 4 microcontroller pins

- IR Remote Control Receiver

In this lab students are required to design and implement IR remote control receiver using AVR 8515 microcontroller.

- Step Motor Controller

In this lab students are meant to implement a compact size and high-speed interrupt driven step motor controller.

- A Temperature Monitoring and Acquisition System with LCD Output and memory interface

Implement this using the SDK- 500 Kit for AVR.

7. DESIGNING WITH FPGAS - LAB

- USART

Designing the Specifications and circuit of a usart.
Implementation of a USART on FPGA.

- Multiplexed Display Controller

Designing the Specifications and circuit of a Multiplexed Display Controller (MDC)
Implementation of a Multiplexed Display Controller on FPGA.

- CRT Controller

Designing the Specifications and circuit of a CRT Controller.
Implementation of a CRT Controller on FPGA.

- I/O Port Expander

Designing the Specifications and circuit of I/O port expander .
Implementation of I/O Expander on FPGA.

- Scanned Keyboard Controller

Designing the Specifications and circuit of a Scanned Keyboard Controller.
Implementation of a Scanned Keyboard Controller on FPGA.

- Filter Implementation using MAC

Designing the Specifications and circuit of a Filter Implementation using MAC.
Implementation of a MAC on FPGA.

SEMESTER 3

E1: SYSTEM ON CHIP (SOC):

- System on Chip Technology Challenges
- System On a Chip (SOC) components.
- SoC Design Methodology
- Parameterized Systems-on-a-Chip
- System-on-a-chip Peripheral Cores
- SoC and interconnect centric Architectures
- System level design representations and modeling languages.
- Target architecture models.
- Intra-chip communication.
- Graph partitioning algorithms.
- Task time measurement.
- Interconnect latency modeling.
- Back annotation of lower level timing to high-level models.
- Synthesis of SOC components.
- System Level, Block Level and Hardware/Software Co-verification
- SOC components: emulation, co-simulation, Physical Verification.

Text/References

- Wayone Wolf," Modern VLSI Design: SOC Design"
- Prakash Rashnikar, Peter Paterson, Lenna Singh" System-On-A-Chip Verification methodlogy & Techniques", Kluwer Academic Publishers.
- Alberto Sangiovanni Vincentelli," Surviving the SOC Revolution: A Guide to Platform-based Design", Kluwer Academic Publishers.

E2: SENSOR TECHNOLOGIES AND MEMS:

- Sensors types and classification – mechanical, acoustic, magnetic, thermal, chemical, radiation and biosensors. Microsensors.
- Sensors based on surface-acoustic wave devices.
- Micromachining techniques
- MEMS for automative, communication and signal processing applications.
- Modeling and simulation of microsensors and actuators.
- Sensors and smart structures.
- Micro-opto-electro-mechanical sensors and system.

Text /References

- Ristic L (ed), "Sensor Technology and Devices", Artech House, London, 1994.
- Sze S.M. (ed), "Semiconductor Sensors", John Wiley, New York, 1994 Wise
- K.D. (Guest Editor) "Integrated Sensors, Microp-actuators and micro-systems (MEMS)", Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998.

E3:PROCESS AND DEVICE CHARACTERIZATION & MEASUREMENTS:

- Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR

- Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope
- Material and Impurity Characterization: SIMS, XRD, EDAX
- Electrical Characterization:
- our-probe technique, Hall effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements
- Process and SPICE model parameter Extraction.

Text /References

- W.R. Reunyan, " Semiconductor Measurements And Instrumentation", Mc-Graw Hill.
- Schroder, "Semiconductor Material And Device Characterization"
- Philips F. Kare and Greydon B. Lauabee, " Characterization of semiconductor Materials", Mc-Graw Hill.
- K.V. Ravi, "Imperfections And Impurities In Semiconductor Silicon", John Wiley And Sons.

E4: RF DESIGN:

- Introduction to RF Electronics.
- Basic concepts in RF design.
- MOS Review
- Path Loss
- Small Signal Model
- Receiver Design
- RF Transreceivers
- Low Noise RF amplifiers and Mixers.
- RF Power amplifiers.
- RF Oscillators.

Text/References

- Behzad Razavi, "RF Microelectronics", Pearson Education.
- Reinhold Ludwig, Paul Bretchko,"RF Circuit Design: Theory & Applications "
- Peter b. Kenington, "High Linearity RF Amplifier Design ", Artech House Microwave Library.
- Jeremy Everard, "Fundamentals of RF Circuit Design With Low Noise Oscillators", John Wiley & Sons Ltd.

E5: OPTICAL COMMUNICATION:

Basic elements of optical systems- mirrors, gratings, lenses. Transducers- spatial light modulators, Holographic elements, Fundamental Limitations on dynamic range, Hybrid optical electronics systems, Dependence between optics and electronics.Image spectral analysis and filtering, pattern recognitions Picture deblurring –synthetic aperture Radar imaging. Radio signal analysis-simple arithmetic, matrix operation- Differential and integration

Non –linear effects- optical bistability, Hybrid polarisation devices, optical phase conjugation. Passive and Active integrated optic devices

Digital optical computers – Internal representation, implementation of binary logic elements, implementation of arithmetic units.

Memory – interconnection and communication –Architectures

Text /References

- Optical Computing: An Introduction by Mohammad A. Karim, Abdul A. S. Awwal
- A Digital Design Methodology for Optical Computing by Miles Murdocca
- Introduction to Fourier Optics by Joseph W. Goodman
- Feitelson, D. G., Optical Computing: A Survey for Computer Scientists., (ISBN 0-262-061-120), MIT Press 1988.

E6: DESIGN FOR RELIABILITY

Review of probability theory, nature of reliability problems in electronics equipments, reliability modeling, fault analysis technique, reliability predictions, software reliability, introduction to state space analysis.

Text /References

- Design Reliability: Fundamentals and Applications - by Balbir S. Dhillon
- Reliability: Modeling, Prediction, and Optimization by Wallace R. Blischke, D. N. Prabhakar Murthy
- Reliability: Modeling, Prediction, and Optimization

E7: Integrated Optics and Optical Networks:

- Introduction: Review of light propagation, Optical fiber characterization, Cable design and connectors, Bragg gratings, LED and LASER device structures, detector terminology, and characteristics.
- Integrated Optics: Introduction, Modes in an asymmetric waveguide, ray analysis of planar waveguide, WKB analysis of inhomogeneous planar waveguides, Strip waveguides, Guided wave devices: Phase modulator, Mach-Zehdner interferometer modulator and switch, optical directional coupler, comparison of bulk and integrated optical modulators.
- Broadband circuits for Optical Fiber Communication: Main Amplifier circuit and Driver circuit implementations: MESFET, HFET, BJT, HBT, CMOS Technology
- Optical Networking: Optical Wavelength Division Multiplexing, Commercial WDM systems, Intelligent Optical internetworking, Architecture, Tunable transmitters and receivers, Optical Amplifier, Wavelength multiplexer/demultiplexer, Wavelength Routers, Wavelength Converters , Applications: Asynchronous Transmitter Mode (ATM) and Synchronous Optical Network(SONET).

Text /References

- Govind P. Agarwal: Fiber Optic Communication Systems, 2nd Edition (John Wiley)
- Casimer DeCusatis: Fiber Optic Data Communication: Technological trends and advances (Academic Press)
- Optical Electronics: Ajoy Ghatak and K. Thyagarajan (Cambridge University Press)
- Gray and Meyer: Analysis and Design of Analog Integrated Circuits
- John Gowar: Optical Communication System, 2nd Edition, Prentice Hall India
- Wireless Optical Communication Systems: Steve Hranilovic: Springer
- Das : Optical Signal Processing, Springer – Verlag 1990

SEMESTER 4

Thesis work

Thesis work will start from the 3rd semester and will continue in the 4th semester.